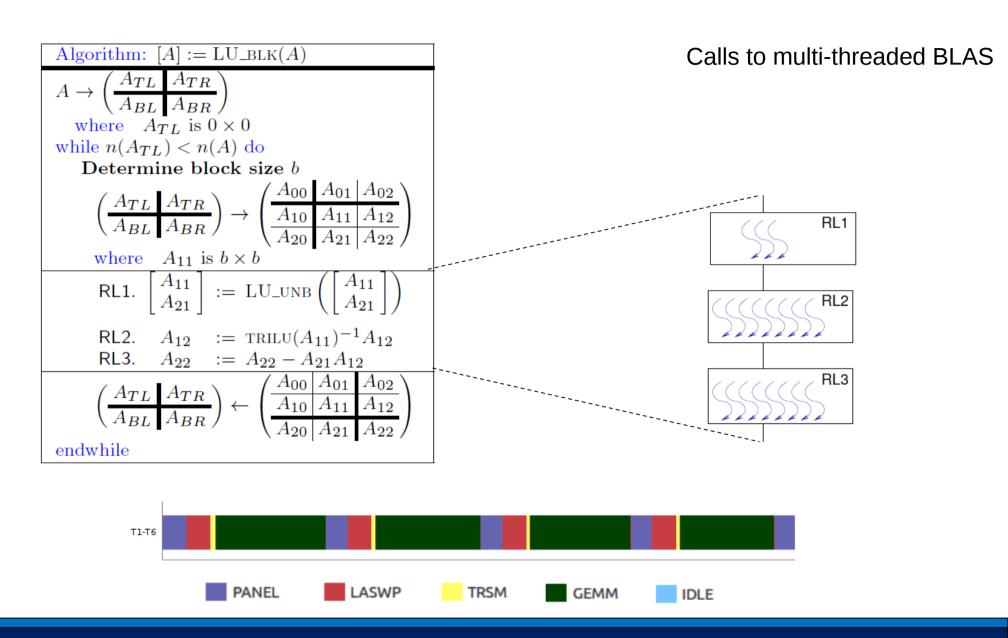
# A Case for Malleable Thread-Level Linear Algebra Libraries: The LU Factorization with Partial Pivoting

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## The LU factorization (Right-looking variant)



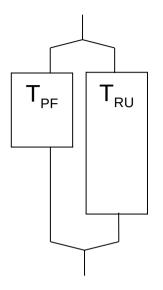


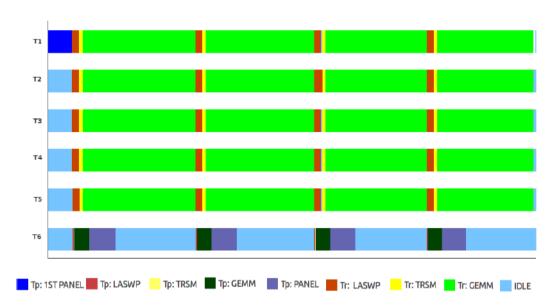
# Look-ahead to overlap RL1 with remaining kernels

| Algorithm: 
$$[A] := LU_{LA_BLK}(A)$$
 | Determine block size  $b$  |  $A \to \begin{pmatrix} A_{TL} & A_{TR} \\ A_{BL} & A_{BR} \end{pmatrix}$ ,  $A_{BR} \to \begin{pmatrix} A_{BR} & A_{BR} \\ A_{BL} & A_{BR} \end{pmatrix}$ ,  $A_{BR} \to \begin{pmatrix} A_{BR} & A_{BR} \\ A_{BL} & A_{BR} \end{pmatrix}$ ,  $A_{BR} \to k$  columns  $A_{BR}^P := LU_{LUNB}(A_{BR}^P)$  | while  $n(A_{TL}) < n(A)$  do |  $A_{01} & A_{02} \\ A_{10} & A_{11} & A_{12} \\ A_{20} & A_{21} & A_{22} \end{pmatrix}$  | where  $A_{11}$  is  $b \times b$  | Determine block size  $b$  | % Partition into panel factorization and remainder |  $\begin{pmatrix} A_{12} & A_{12} \\ A_{22} & A_{22} \end{pmatrix} \to \begin{pmatrix} A_{12}^P & A_{12}^P \\ A_{22}^P & A_{22}^P & A_{22}^P \end{pmatrix}$  | where both  $A_{12}^P$ ,  $A_{22}^P$  have  $b$  columns | FF1 |  $A_{12}^P$  |

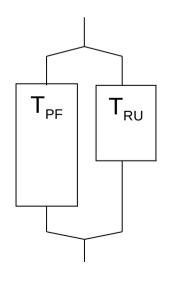


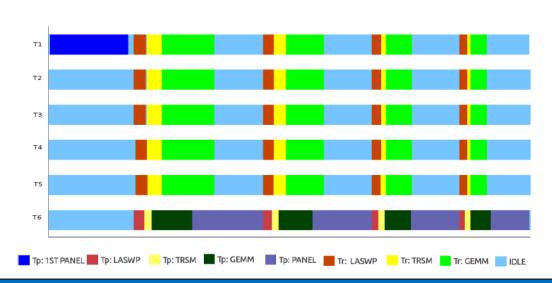
#### T<sub>RU</sub>>T<sub>PF</sub>: Malleable BLIS





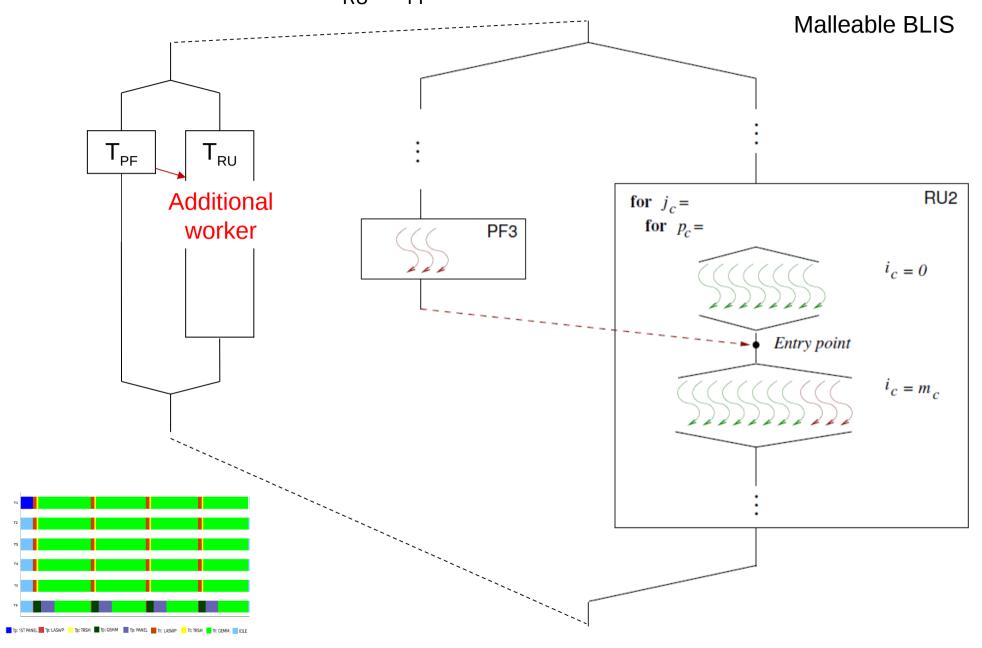
 $T_{PF}>T_{RU}$ : Early Termination (ET)





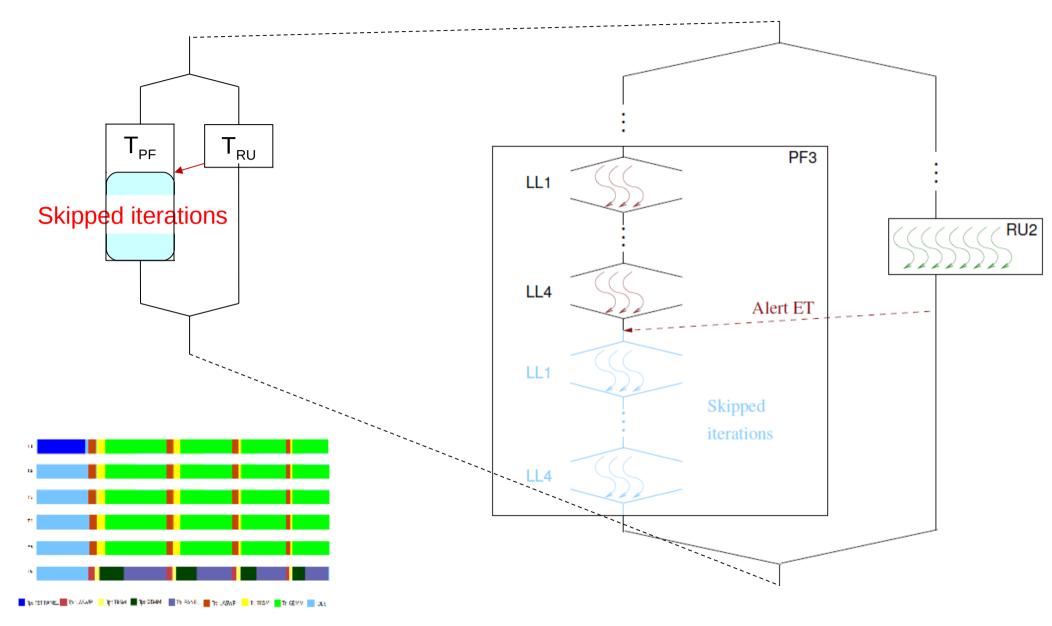


#### T<sub>RU</sub>>T<sub>PF</sub>: Malleable BLIS





### $T_{PF}>T_{RU}$ : Early Termination (ET)





#### **Experimental evaluation**

LU on Intel Xeon E5-2603 v3

